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10EC63

Sixth Semester B.E. Degree Examination, Dec.2014/Jan.2015
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

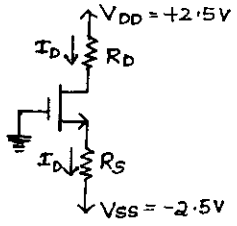
Note: ***Answer any FIVE full questions, selecting atleast THREE questions from Part-A and TWO from Part-B.***

PART – A

1 a. Derive an expression for drain current of a MOSFET in different regions of operation. **(06 Marks)**

b. Design a circuit of Fig.Q.1(b), so that the transistor operates at $I_D = 0.4mA$ and $V_D = +0.5V$. The NMOS transistor has $V_t = 0.7V$, $\mu_n C_{ox} = 100\mu A/V^2$, $L = 1\mu m$, and $W = 32\mu m$. Neglect channel length modulation effect ($\lambda = 0$). **(04 Marks)**

Fig.Q.1(b)



c. Draw the small signal circuit model of MOSFET when $|VSB| \neq 0$ and explain briefly. (ie including the body effect). **(04 Marks)**

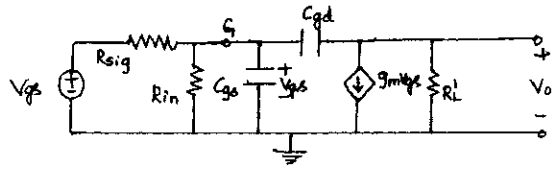
d. For the common drain amplifier stage, draw the small signal equivalent circuit and drive expressions for A_v, A_{vo}, G_v, R_{in} and R_{out}. **(06 Marks)**

2 a. Compare and explain the important characteristics of NMOS and NPN transistors. **(05 Marks)**

b. With a neat circuit diagram and equations explain the basic BJT current steering circuits. **(05 Marks)**

c. For the high frequency equivalent circuit of common source amplifier in Fig.Q.2(c), find the midband voltage gain $A_m = V_o/V_{sig}$ and upper 3dB frequency f_H using open circuit time constants. **(08 Marks)**

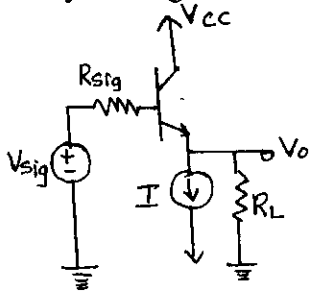
Fig.Q.2(c)



Where $R_L' = 3.3K\Omega$; $R_{sig} = 100K\Omega$; $R_{in} = 420K\Omega$; $C_{gs} = C_{gd} = 1P_f$, $g_m = 4m$ A/V.

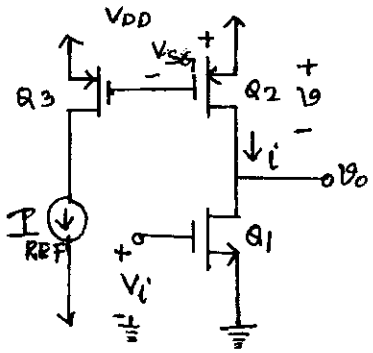
d. For the emitter follower biased by a constant current source I, shown in Fig.Q.2(d), draw the high frequency equivalent circuit clearly naming all the components: **(02 Marks)**

Fig.Q.2(d)



3 a. A CMOS common source amplifier shown in Fig.Q.3(a) is fabricated with W/L = 100 μm/1.6 μm for all transistors. With Kn′ = 90 μA/V², Kp1′ = 30 μA/V², IREF = 100μA, V_{An} = 8 V/μm and V_{AP} = 12 V/μm, determine the following quantities g_{m1}, r_{o1}, r_{o2}, A_{vo}. **(06 Marks)**

Fig.Q.3(a)



b. Draw the MOS cascade amplifier circuit with current source biasing. With the help of small signal equivalent circuit. Show that the cascading increases magnitude of open circuit voltage gain from A_o to A_o^2. **(06 Marks)**

c. Write short notes on cascade MOS current mirror circuit. **(04 Marks)**

d. Find A_o for an NMOS transistor fabricated in a 0.4μm CMOS process for which Kn′ = 200μA/V², and VA′ = 20V/μm. The transistor has a 0.4μm channel length and is operated with an overdrive voltage of 0.25V. What must be W for NMOS transistor to operate at I_D = 100μA? Also find r_o and g_m. **(04 Marks)**

4 a. Explain the operation of MOS differential pair with a differential input voltage and derive the range of differential input for differential mode of operation. **(08 Marks)**

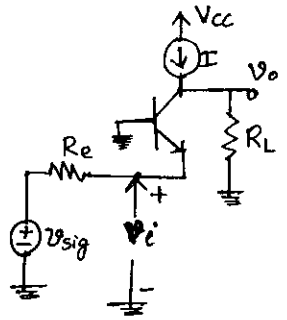
b. Prove that $A_{CM} = \frac{-r_{o4}}{2R_{SS}} \times \frac{1}{1+g_{m3}\,r_{03}}$ for the active loaded MOS differential amplifier. **(08 Marks)**

c. For the BJT differential amplifier having β = 100, matched to 10% or better, and areas that are matched to 10% or better, along with collector resistors that are matched to 2% or better, find V_{OS}, I_B and I_{OS}. The dc bias current is 100μA. **(04 Marks)**

5 a. Explain the operation of MOSFET as a linear amplifier. **(05 Marks)**

b. For the common base amplifier shown in Fig.Q.5(b) draw the small signal equivalent circuit and hence derive an expression for R_{in}, R_{out} and A_{vo}. **(06 Marks)**

Fig.Q.5(b)



c. A MOS differential amplifier is operated at a total current of 0.8mA, using transistors with W/L ratios of 100, $K_n' = \mu_n C_{ox}$ = 0.2 mA/V², V_A = 20V and R_D = 5KΩ. Find $V_{OV} = (V_{GS} - V_t)$, g_m, r_o, A_d. **(05 Marks)**

d. Explain channel length modulation effect of MOSFET. **(04 Marks)**

PART – B

6 a. What are the four properties of negative feed back? Briefly explain about each property. **(08 Marks)**

b. For the series-shunt feedback ideal amplifier find A_f, R_{if} and R_{of}. **(06 Marks)**

c. Discuss the method of frequency compensation for modifying open loop gain A(s) so that the closed loop amplifier is stable, by introducing a new pole in transfer function at sufficiently low frequency. **(06 Marks)**

7 a. Draw the circuit diagram of basic difference amplifier and derive an expression for the output voltage V_{out} and differential input resistance R_{id}. **(05 Marks)**

b. Show that the gain bandwidth product of an inverting amplifier is smaller than that of a non inverting amplifier. **(05 Marks)**

c. Find the output voltage of the circuit, assuming Op. Amp M1 has DC open loop gain of 1×10^5 and a bandwidth of 10 rad/sec., op amp M_2 is an ideal op. amp (Ref.Fig.Q.7(c)). **(06 Marks)**

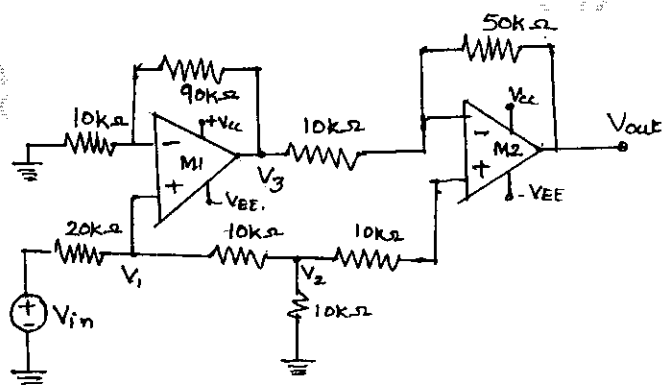


Fig.Q.7(c)

d. Write a note on use of op-amp in sample and hold circuit. **(04 Marks)**

8 a. Draw the basic structure of CMOS inverter and explain the voltage transfer characteristic of CMOS inverter **(08 Marks)**

b. Consider a CMOS inverter fabricated in a 0.25μm process for which $C_{ox} = 6fF/\mu m^2$, $\mu_n C_{ox} = 115\mu A/V^2$, $\pi_p C_{ox} = 30\mu A/V^2$, $V_{tn} = -V_{tp} = 0.4V$ and $V_{DD} = 2.5V$. The W/L ratio of Q_N is 0.375 μm/0.25μm and for Q_p is 1.125μm/0.25μm. The equivalent capacitance value is 6.25fF. Find t_{PHL}, t_{PLH} and t_p. **(06 Marks)**

c. Explain with neat circuit diagrams about pull-up and pull-down networks used in CMOS logic circuits. **(06 Marks)**

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